

## CLAIMS

### What is claimed is:

- 1 1. A networking apparatus comprising:
  - 2 a switching fabric including a plurality of ingress/egress points to switch
  - 3 routing paths of packets received through mediums coupled to the ingress/egress
  - 4 points;
  - 5 a first buffering structure including a first plurality of storage structures and
  - 6 first associated packet diversion and insertion logic, coupled to a first of said
  - 7 ingress/egress point to facilitate at least a selected one of diversion of selected ones
  - 8 of a first plurality of egress packets being routed through said first ingress/egress
  - 9 point onto a first one of said mediums, and insertion of additional ones into said first
  - 10 plurality of egress packets being routed; and
  - 11 a second buffering structure including a second plurality of storage structures
  - 12 and second associated packet diversion and insertion logic, coupled to a second of
  - 13 said ingress/egress points to facilitate at least a selected one of diversion of selected
  - 14 ones of a second plurality of egress packets being routed through said second
  - 15 ingress/egress point onto a second one of said mediums, and insertion of additional
  - 16 ones into said second plurality of egress packets being routed.
- 1 2. The apparatus of claim 1, wherein said first buffering structure comprises
  - 2 a first storage structure to stage undiverted ones of said egress packets;
  - 3 a second storage structure to stage diverted ones of said egress packets;
  - 4 a divert logic coupled to the first ingress/egress point and said first and
  - 5 second storage structures to selective route said egress packets from said first

6 ingress/egress point onto a selected one of said first and second storage structures;

7 and

8 a register interface, including packet unpacking logic, coupled to the second

9 storage structure to facilitate retrieval by a processor said diverted ones of said

10 egress packets in unpacked portions.

1 3. The apparatus of claim 1, wherein said first buffering structure comprises

2 a first storage structure coupled to the first ingress/egress point to stage

3 undiverted ones of said egress packets;

4 a second storage structure to stage insertion ones of said egress packets;

5 a register interface, including packet packing logic, to facilitate provision to

6 said second storage structure by a processor said insertion ones of said egress

7 packets in unpacked portions; and

8 an insertion logic coupled to the first and second storage structures to

9 selective merge said undiverted ones and said insertion ones of said egress

10 packets.

1 4. The apparatus of claim 1, wherein said first buffering structure further

2 facilitates at least an additional selected one of diversion of selected ones of a first

3 plurality of ingress packets being received from said first medium into said switching

4 fabric through said first ingress/egress point, and insertion of additional ones into

5 said first plurality of ingress packets being received.

1 5. The apparatus of claim 4, wherein said first buffering structure comprises

2 a first storage structure to stage undiverted ones of said ingress packets;

3 a second storage structure to stage diverted ones of said ingress packets;

4           a divert logic coupled to the first medium and said first and second storage  
5        structures to selective route said ingress packets received from said first medium  
6        onto a selected one of said first and second storage structures; and  
7           a register interface, including packet unpacking logic, coupled to the second  
8        storage structure to facilitate retrieval by a processor said diverted ones of said  
9        ingress packets in unpacked portions.

1   6.    The apparatus of claim 4, wherein said first buffering structure comprises  
2        a first storage structure coupled to the first medium to stage undiverted ones  
3        of said ingress packets;

4        a second storage structure to stage insertion ones of said ingress packets;  
5        a register interface, including packet packing logic, to facilitate provision to  
6        said second storage structure by a processor said insertion ones of said ingress  
7        packets in unpacked portions; and  
8           an insertion logic coupled to the first and second storage structures to  
9        selective merge said undiverted ones and said insertion ones of said ingress  
10      packets.

1   7.    The apparatus of claim 4, wherein said second buffering structure further  
2        facilitates at least an additional selected one of diversion of selected ones of a  
3        second plurality of ingress packets being received from said second medium into  
4        said switching fabric through said second ingress/egress point, and insertion of  
5        additional ones into said second plurality of ingress packets being received.

1 8. A networking apparatus comprising:  
2       a switching fabric including a plurality of ingress/egress points to switch  
3       routing paths of packets received through mediums coupled to the ingress/egress  
4       points;  
5       a first buffering structure including a first plurality of storage structures and  
6       first associated packet diversion and insertion logic, coupled to a first of said  
7       ingress/egress points to facilitate at least a selected one of diversion of selected  
8       ones of a first plurality of ingress packets being received from a first one of said  
9       mediums into said switching fabric through said first ingress/egress point, and  
10      insertion of additional ones into said first plurality of ingress packets being received;  
11      and  
12      a second buffering structure including a second plurality of storage structures  
13      and second associated packet diversion and insertion logic, coupled to a second of  
14      said ingress/egress points to facilitate at least a selected one of diversion of selected  
15      ones of a second plurality of ingress packets being received from a second one of  
16      said mediums into said switching fabric through said second ingress/egress point,  
17      and insertion of additional ones into said second plurality of ingress packets being  
18      received.

1 9. The apparatus of claim 8, wherein said first buffering structure comprises  
2       a first storage structure to stage undiverted ones of said ingress packets;  
3       a second storage structure to stage diverted ones of said ingress packets;  
4       a divert logic coupled to the first medium and said first and second storage  
5       structures to selective route said ingress packets received from said first medium  
6       onto a selected one of said first and second storage structures; and

7           a register interface, including packet unpacking logic, coupled to the second  
8   storage structure to facilitate retrieval by a processor said diverted ones of said  
9   ingress packets in unpacked portions.

1   10.   The apparatus of claim 8, wherein said first buffering structure comprises  
2       a first storage structure coupled to the first medium to stage undiverted ones  
3   of said ingress packets;

4       a second storage structure to stage insertion ones of said ingress packets;  
5       a register interface, including packet packing logic, to facilitate provision to  
6   said second storage structure by a processor said insertion ones of said ingress  
7   packets in unpacked portions; and

8       an insertion logic coupled to the first and second storage structures to  
9   selective merge said undiverted ones and said insertion ones of said ingress  
10   packets.

1   11.   A networking apparatus comprising:  
2       a switching fabric including a plurality of ingress/egress points to switch  
3   packets received through mediums coupled to the ingress/egress points; and  
4       a buffering structure including  
5       a first plurality of storage structures and first associated packet diversion  
6       and insertion logic, coupled to a first of said ingress/egress points, to  
7   facilitate at least a selected one of diversion of selected ones of a  
8       plurality of ingress packets being received from a first one of said  
9       mediums into said switching fabric through said first ingress/egress  
10      point, and insertion of additional ones into said plurality of ingress  
11      packets being received, and

12                   a second buffering structure including a second plurality of storage  
13                   structures and second associated packet diversion and insertion logic,  
14                   coupled to the first ingress/egress point, to facilitate at least a selected  
15                   one of diversion of selected ones of a plurality of egress packets being  
16                   routed through said first ingress/egress point onto said first medium,  
17                   and insertion of additional ones into said plurality of ingress packets  
18                   being routed.

1   12. The apparatus of claim 11, wherein said first plurality of storage structures  
2   and associated first packet diversion and insertion logic comprises  
3                   a first storage structure to stage undiverted ones of said egress packets;  
4                   a second storage structure to stage diverted ones of said egress packets;  
5                   a divert logic coupled to the first ingress/egress point and said first and  
6                   second storage structures to selective route said egress packets from said first  
7                   ingress/egress point onto a selected one of said first and second storage structures;  
8                   and  
9                   a register interface, including packet unpacking logic, coupled to the second  
10                  storage structure to facilitate retrieval by a processor said diverted ones of said  
11                  egress packets in unpacked portions.

1   13. The apparatus of claim 11, wherein said first plurality of storage structures  
2   and associated first packet diversion and insertion logic comprises  
3                   a first storage structure coupled to the first ingress/egress point to stage  
4                   undiverted ones of said egress packets;  
5                   a second storage structure to stage insertion ones of said egress packets;

6           a register interface, including packet packing logic, to facilitate provision to  
7    said second storage structure by a processor said insertion ones of said egress  
8    packets in unpacked portions; and

9           an insertion logic coupled to the first and second storage structures to  
10   selective merge said undiverted ones and said insertion ones of said egress  
11   packets.

1   14.   The apparatus of claim 11, wherein said second plurality of storage structures  
2   and associated second packet diversion and insertion logic comprises

3           a first storage structure to stage undiverted ones of said ingress packets;  
4           a second storage structure to stage diverted ones of said ingress packets;  
5           a divert logic coupled to the first medium and said first and second storage  
6   structures to selective route said ingress packets received from said first medium  
7   onto a selected one of said first and second storage structures; and

8           a register interface, including packet unpacking logic, coupled to the second  
9   storage structure to facilitate retrieval by a processor said diverted ones of said  
10   ingress packets in unpacked portions.

1   15.   The apparatus of claim 11, wherein said second plurality of storage structures  
2   and associated second packet diversion and insertion logic comprises

3           a first storage structure coupled to the first medium to stage undiverted ones  
4   of said ingress packets;

5           a second storage structure to stage insertion ones of said ingress packets;  
6           a register interface, including packet packing logic, to facilitate provision to  
7    said second storage structure by a processor said insertion ones of said ingress  
8   packets in unpacked portions; and

9           an insertion logic coupled to the first and second storage structures to  
10    selective merge said undiverted ones and said insertion ones of said ingress  
11    packets.

1    16.   An optical networking module comprising:  
2           an optical component to send and receive optical signals encoded with data  
3    transmitted through a coupled optical medium;  
4           an optical-electrical component coupled to the optical component to encode  
5    digital data onto optical signals and to decode encoded digital data on optical signals  
6    back into their digital forms;  
7           a data link/physical layer processing unit, including a buffering structure  
8    comprising a plurality of storage structures and associated packet diversion and  
9    insertion logic, coupled to the optical-electrical component and to a packet  
10   source/sink, to facilitate at least a selected one of data link/physical processing of  
11   ingress packets received from said optical medium for said packet source/sink and  
12   egress packets to be routed from said packet source/sink onto said optical medium,  
13   with each of said data link/physical processing of ingress and egress packets  
14   including at least a selected one of diversion of selected ones of a plurality of  
15   ingress/egress packets being received from/routed onto said optical medium, and  
16   insertion of additional ones into said plurality of ingress/egress packets being  
17   received/routed; and  
18           a body encasing said optical component, said optical-electrical component,  
19    and said data link/physical processing unit as a single module.

1    17.   The optical networking module of claim 16, wherein said plurality of storage  
2    structures and associated packet diversion and insertion logic comprises  
3           a first storage structure to stage undiverted ones of said egress packets;

4           a second storage structure to stage diverted ones of said egress packets;  
5           a divert logic coupled to said packet source/sink and said first and second  
6   storage structures to selectively route said egress packets from said packet  
7   source/sink onto a selected one of said first and second storage structures; and  
8           a register interface, including packet unpacking logic, coupled to the second  
9   storage structure to facilitate retrieval by a processor said diverted ones of said  
10 egress packets in unpacked portions.

1   18.   The optical networking module of claim 16, wherein said plurality of storage  
2   structures and associated packet diversion and insertion logic comprises  
3           a first storage structure coupled to the packet source/sink to stage undiverted  
4   ones of said egress packets;  
5           a second storage structure to stage insertion ones of said egress packets;  
6           a register interface, including packet packing logic, to facilitate provision to  
7   said second storage structure by a processor said insertion ones of said egress  
8   packets in unpacked portions; and  
9           an insertion logic coupled to the first and second storage structures to  
10 selective merge said undiverted ones and said insertion ones of said egress  
11 packets.

1   19.   The optical networking module of claim 16, wherein said plurality of storage  
2   structures and associated packet diversion and insertion logic comprises  
3           a first storage structure to stage undiverted ones of said ingress packets;  
4           a second storage structure to stage diverted ones of said ingress packets;  
5           a divert logic coupled to the optical medium and said first and second storage  
6   structures to selective route said ingress packets received from said optical medium  
7   onto a selected one of said first and second storage structures; and

8           a register interface, including packet unpacking logic, coupled to the second  
9   storage structure to facilitate retrieval by a processor said diverted ones of said  
10   ingress packets in unpacked portions.

1   20.   The optical networking module of claim 16, wherein said plurality of storage  
2   structures and associated packet diversion and insertion logic comprises  
3        a first storage structure coupled to the optical medium to stage undiverted  
4   ones of said ingress packets;  
5        a second storage structure to stage insertion ones of said ingress packets;  
6        a register interface, including packet packing logic, to facilitate provision to  
7   said second storage structure by a processor said insertion ones of said ingress  
8   packets in unpacked portions; and  
9        an insertion logic coupled to the first and second storage structures to  
10   selective merge said undiverted ones and said insertion ones of said ingress  
11   packets.

1   21.   The optical network module of claim 16, wherein said optical and optical-  
2   electrical components, said data link/physical layer processing unit are all designed  
3   to support data rates of at least 10GB/s.

1  
1   22.   The optical network module of claim 16, wherein said data link/physical layer  
2   processing unit is a multi-protocol processor that supports a plurality of datacom and  
3   telecom protocols.

1 23. A multi-protocol processor comprising:  
2       a plurality of I/O interfaces to facilitate selective optical-electrical trafficking of  
3 data transmitted in accordance with a selected one of a plurality of datacom and  
4 telecom protocols;  
5       a plurality of data link and physical sub-layer processing units selectively  
6 coupled to each other and to the I/O interfaces to be selectively employed in  
7 combination to perform selected data link and physical sub-layer processing on  
8 egress as well as ingress ones of said data, in accordance with said selected one of  
9 said plurality of protocols; and  
10      a buffering structure coupled to at least a system-side one of said I/O  
11 interfaces and a media processing one of said data link and physical sub-layer  
12 processing units, including a plurality of storage structures and associated packet  
13 diversion and insertion logic to facilitate at least a selected one of diversion of  
14 selected ones of a plurality of egress packets, and insertion of additional ones into  
15 said plurality of egress packets, diversion of selected ones of a plurality of ingress  
16 packets, and insertion of additional ones into said plurality of ingress packets. .

1 24. The processor of claim 23, wherein said plurality of storage structures and  
2 associated packet diversion and insertion logic comprises  
3       a first storage structure to stage undiverted ones of said egress packets;  
4       a second storage structure to stage diverted ones of said egress packets;  
5       a divert logic coupled to said packet source/sink and said first and second  
6 storage structures to selectively route said egress packets from said packet  
7 source/sink onto a selected one of said first and second storage structures; and

8           a register interface, including packet unpacking logic, coupled to the second  
9   storage structure to facilitate retrieval by a processor said diverted ones of said  
10 egress packets in unpacked portions.

1   25.   The processor of claim 23, wherein said plurality of storage structures and  
2   associated packet diversion and insertion logic comprises  
3        a first storage structure coupled to the packet source/sink to stage undiverted  
4   ones of said egress packets;  
5        a second storage structure to stage insertion ones of said egress packets;  
6        a register interface, including packet packing logic, to facilitate provision to  
7   said second storage structure by a processor said insertion ones of said egress  
8   packets in unpacked portions; and  
9        an insertion logic coupled to the first and second storage structures to  
10 selective merge said undiverted ones and said insertion ones of said egress  
11 packets.

1   26.   The processor of claim 23, wherein said plurality of storage structures and  
2   associated packet diversion and insertion logic comprises  
3        a first storage structure to stage undiverted ones of said ingress packets;  
4        a second storage structure to stage diverted ones of said ingress packets;  
5        a divert logic coupled to the optical medium and said first and second storage  
6   structures to selective route said ingress packets received from said optical medium  
7   onto a selected one of said first and second storage structures; and  
8        a register interface, including packet unpacking logic, coupled to the second  
9   storage structure to facilitate retrieval by a processor said diverted ones of said  
10 ingress packets in unpacked portions.

1 27. The processor of claim 23, wherein said plurality of storage structures and  
2 associated packet diversion and insertion logic comprises  
3 a first storage structure coupled to the optical medium to stage undiverted  
4 ones of said ingress packets;  
5 a second storage structure to stage insertion ones of said ingress packets;  
6 a register interface, including packet packing logic, to facilitate provision to  
7 said second storage structure by a processor said insertion ones of said ingress  
8 packets in unpacked portions; and  
9 an insertion logic coupled to the first and second storage structures to  
10 selective merge said undiverted ones and said insertion ones of said ingress  
11 packets.

1 28. The processor of claim 23, wherein said interfaces, said plurality of data link  
2 and physical sub-layer processing units and said buffering structure are all designed  
3 to support data rates of at least 10GB/s.

1 29. The processor of claim 23, wherein said processor is disposed on a single  
2 integrated circuit.

1 30. A buffering structure comprising:  
2 a first storage structure to stage undiverted ones of egress packets;  
3 a second storage structure to stage diverted ones of egress packets;  
4 a third storage structure to stage insertion ones of egress packets;  
5 a first divert logic coupled to said first and second storage structures to  
6 selectively route egress packets onto a selected one of said first and second storage  
7 structures;

1           a first insert logic coupled to said first and third storage structures to  
2 selectively merge said undiverted ones and said insertion ones of said egress  
3 packets; and  
4           a register interface, including packet packing and unpacking logic, coupled to  
5 the second and third storage structures to facilitate retrieval by a processor said  
6 diverted ones of said egress packets in unpacked portions, and provision by said  
7 processor said insertion ones of said egress packets in unpacked portions.

1   31. The buffering structure of claim 30, wherein said buffering structure further  
2 comprises

3           a fourth storage structure to stage undiverted ones of ingress packets;  
4           a fifth storage structure to stage diverted ones of ingress packets;  
5           a second divert logic coupled to said fourth and fifth storage structures to  
6 selective route ingress packets onto a selected one of said fourth and fifth storage  
7 structures; and  
8           said register interface, also coupled to the fifth storage structure to facilitate  
9 retrieval by said processor said diverted ones of said ingress packets in unpacked  
10 portions.

1   32. The buffering structure of claim 30, wherein  
2        said buffering structure further comprises  
3           a fourth storage structure to stage undiverted ones of ingress packets,  
4           a fifth storage structure to stage insertion ones of ingress packets, and  
5           an insertion logic coupled to the fourth and fifth storage structures to  
6           selective merge said undiverted ones and said insertion ones of said  
7           ingress packets; and

8           said register interface is further coupled to said fifth storage structures to  
9   facilitate provision to said fifth storage structure by said processor said insertion  
10   ones of said ingress packets in unpacked portions.

1   33.   A buffering structure comprising:  
2           a first storage structure to stage undiverted ones of ingress packets;  
3           a second storage structure to stage diverted ones of ingress packets;  
4           a third storage structure to stage insertion ones of ingress packets;  
5           a first divert logic coupled to said first and second storage structures to  
6   selectively route ingress packets onto a selected one of said first and second  
7   storage structures;  
8           a first insert logic coupled to said first and third storage structures to  
9   selectively merge said undiverted ones and said insertion ones of said ingress  
10   packets; and  
11           a register interface, including packet packing and unpacking logic, coupled to  
12   the second and third storage structures to facilitate retrieval by a processor said  
13   diverted ones of said ingress packets in unpacked portions, and provision by said  
14   processor said insertion ones of said ingress packets in unpacked portions.

1   34.   The buffering structure of claim 33, wherein said buffering structure further  
2   comprises  
3           a fourth storage structure to stage undiverted ones of egress packets;  
4           a fifth storage structure to stage diverted ones of egress packets;  
5           a second divert logic coupled to said fourth and fifth storage structures to  
6   selective route egress packets onto a selected one of said fourth and fifth storage  
7   structures; and

8        said register interface, also coupled to the fifth storage structure to facilitate  
9    retrieval by said processor said diverted ones of said egress packets in unpacked  
10   portions.

1    35.   The buffering structure of claim 33, wherein  
2        said buffering structure further comprises  
3            a fourth storage structure to stage undiverted ones of egress packets,  
4            a fifth storage structure to stage insertion ones of egress packets, and  
5            an insertion logic coupled to the fourth and fifth storage structures to  
6            selective merge said undiverted ones and said insertion ones of said  
7            egress packets; and  
8        said register interface is further coupled to said fifth storage structures to  
9    facilitate provision to said fifth storage structure by said processor said insertion  
10   ones of said egress packets in unpacked portions.

1    36.   A buffering structure comprising:  
2            a first storage structure to stage undiverted ones of ingress packets;  
3            a second storage structure to stage diverted ones of ingress packets;  
4            a third storage structure to stage undiverted ones of egress packets;  
5            a fourth storage structure to stage diverted ones of egress packets;  
6            a first divert logic coupled to said first and second storage structures to  
7    selectively route ingress packets onto a selected one of said first and second  
8   storage structures;  
9            a second divert logic coupled to said third and fourth storage structures to  
10   selectively route egress packets onto a selected one of said third and fourth storage  
11   structures; and

1           a register interface, including packet unpacking logic, coupled to the second  
2 and fourth storage structures to facilitate retrieval by a processor said diverted ones  
3 of said ingress and egress packets in unpacked portions.

1   37. The buffering structure of claim 36, wherein  
2        said buffering structure further comprises  
3           a fifth storage structure to stage insertion ones of ingress packets,  
4           an insertion logic coupled to the first and fifth storage structures to  
5           selective merge said undiverted ones and said insertion ones of said  
6           ingress packets; and  
7        said register interface is further coupled to said firth storage structures to  
8        facilitate provision to said fifth storage structure by said processor said insertion  
9        ones of said ingress packets in unpacked portions.

1   38. The buffering structure of claim 36, wherein  
2        said buffering structure further comprises  
3           a fifth storage structure to stage insertion ones of egress packets, and  
4           an insertion logic coupled to the third and fifth storage structures to  
5           selective merge said undiverted ones and said insertion ones of said  
6           egress packets; and  
7        said register interface is further coupled to said firth storage structures to  
8        facilitate provision to said fifth storage structure by said processor said insertion  
9        ones of said egress packets in unpacked portions.

1   39. A buffering structure comprising:  
2        a first storage structure to stage undiverted ones of ingress packets;  
3        a second storage structure to stage insertion ones of ingress packets;

1           a third storage structure to stage undiverted ones of egress packets;  
2           a fourth storage structure to stage insertion ones of egress packets;  
3           a first insertion logic coupled to the first and second storage structures to  
4   selective merge said undiverted ones and said insertion ones of said ingress  
5   packets;  
6           a second insertion logic coupled to the third and fourth storage structures to  
7   selective merge said undiverted ones and said insertion ones of said egress  
8   packets; and  
9           a register interface, including packet packing logic, coupled to the second and  
10   fourth storage structures to facilitate provision by a processor said insertion ones of  
11   said ingress and egress packets in unpacked portions.

1   40.   The buffering structure of claim 39, wherein  
2        said buffering structure further comprises  
3           a fifth storage structure to stage diverted ones of ingress packets,  
4           a divert logic coupled to the first and fifth storage structures to selectively  
5           route ingress packets onto a selected one of said first and fifth storage  
6           structures; and  
7        said register interface is further coupled to said fifth storage structures to  
8   facilitate retrieval by said processor said diverted ones of said ingress packets in  
9   unpacked portions.

1   41.   The buffering structure of claim 39, wherein  
2        said buffering structure further comprises  
3           a fifth storage structure to stage diverted ones of egress packets,

1           a divert logic coupled to the third and fifth storage structures to selectively  
2           route egress packets onto a selected one of said third and fifth storage  
3           structures; and  
4           said register interface is further coupled to said firth storage structures to  
5           facilitate retrieval by said processor said diverted ones of said egress packets in  
6           unpacked portions.

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